

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-28 (canceled).

29. (New) A processor system, comprising:

at least two execution units;

a memory; and

a switch-over unit for switching between at least two operating modes of the processor system, wherein a transition from a first operating mode to a second operating mode of the processor system is triggered by accessing of a predefined memory address.

30. (New) The processor system as recited in Claim 29, further comprising:

a comparator unit, wherein the first operating mode corresponds to a safety mode in which the two execution units redundantly process the same program, and the comparator compares statuses of the two execution units resulting from processing of the same program to determine whether the statuses agree.

31. (New) The processor system as recited in Claim 30, wherein the two execution units synchronously process the same program in the first operating mode.

32. (New) The processor system as recited in Claim 29, wherein the memory includes at least a first, second and third separate memory regions, and wherein in the first operating mode, each execution unit is connected to a respective corresponding area of the first memory region assigned to each execution unit.

33. (New) The processor system as recited in Claim 29, wherein the memory includes at least a first and second separate memory regions, and wherein in the second operating mode, the two execution units are both connected to only the second memory region of the memory assigned to both execution units.

34. (New) The processor system as recited in Claim 33, wherein the predefined memory address is located in the second memory region.

35. (New) The processor system as recited in Claim 29, wherein the memory includes at least a first and second separate memory regions, and wherein in the first operating mode, the two execution units are both connected to only the first memory region of the memory assigned to both execution units.

36. (New) The processor system as recited in Claim 35, wherein the predefined memory address is a trigger address in the first memory region, and wherein a following address, to which access is to be subsequently made, is included in the second memory region.

37. (New) The processor system as recited in Claim 33, wherein the switch-over unit functions as a monitoring unit for monitoring whether the two execution units are connected in the second operating mode only to the second memory region.

38. (New) The processor system as recited in Claim 32, wherein the switch-over unit functions as a monitoring unit for monitoring whether the two execution units are connected in the first operating mode only to the respective corresponding areas of the first memory region.

39. (New) The processor system as recited in Claim 33, wherein each of the memory regions is provided in a separate memory module.

40. (New) The processor system as recited in Claim 30, wherein the comparator is switched off in response to the transition into the second operating mode, and wherein the second operating mode is a performance mode, and wherein a comparison of the statuses of the two execution units takes place only in the first operating mode.

41. (New) The processor system as recited in Claim 29, wherein an interrupt is generated to enable a subsequent return to the first operating mode from the second operating mode.

42. (New) The processor system as recited in Claim 41, wherein the interrupt is triggered by a time condition.

43. (New) The processor system as recited in Claim 41, wherein the interrupt is triggered by a status condition.

44. (New) A method for switching between at least two operating modes of a processor system having at least two execution units and a memory, comprising:

triggering a transition from a first operating mode to a second operating mode of the processor system by the processor system accessing a predefined memory address in the memory.

45. (New) The method as recited in Claim 44, wherein in the first operating mode, the execution units redundantly and synchronously process the same program.

46. (New) The method as recited in Claim 44, wherein different programs are processed in the first and second operating modes, a safety-critical program being redundantly processed by both execution units in the first operating mode, and non-safety-critical programs being processed in the second operating mode.

47. (New) The method as recited in Claim 46, wherein the safety-critical program is redundantly stored in respective memory areas of the first memory region assigned to the two execution units.

48. (New) The method as recited in Claim 46, wherein the non-safety-critical programs are stored in the second memory

region, and wherein both execution units only access the second memory region in the second operating mode.

49. (New) The method as recited in Claim 44, wherein in the first operating mode, the safety-critical program is redundantly processed by the two execution units, and statuses of the two execution units resulting from redundant processing of the safety-critical program are compared for agreement.

50. (New) The method as recited in Claim 44, wherein in the first operating mode, the execution units only access respective memory areas of the first memory region assigned to each execution unit.

51. (New) The method as recited in Claim 44, wherein the memory includes at least a first and second separate memory regions, and wherein in the first operating mode, both execution units access only the first memory region assigned to both execution units.

52. (New) The method as recited in Claims 51, wherein the predefined memory address is a trigger address in the first memory region, and wherein a following address, to which access is to be subsequently made, is included in the second memory region.

53. (New) The method as recited in Claim 44, wherein the memory includes at least a first and second separate memory regions, and wherein in the second operating mode, the two

execution units only access the second memory region assigned to both execution units.

54. (New) The method as recited in Claim 53, further comprising:

monitoring whether the two execution units are only accessing the second memory region in the second operating mode.

55. (New) The method as recited in Claim 51, further comprising:

monitoring whether the two execution units are only accessing the first memory region in the first operating mode.

56. (New) The method as recited in Claim 44, further comprising:

triggering an interrupt based on one of a time condition and a status condition, wherein a transition from the second operating mode to the first operating mode takes place upon triggering of the interrupt.